WHAT IS CLAIMED IS:

1. A light-activated semiconductor switch device, comprising:

a semiconductor switch comprising a first n-doped layer and a first p-doped layer forming a switch blocking junction, a switch axis lying perpendicular to the switch blocking junction, a groove having a light refracting side wall extending into the first n-doped layer from a side of the n-doped layer opposite from the switch blocking junction, at least a portion of the light refracting side wall being disposed non-parallel to the switch plane and to the switch axis.

2. A device as recited in claim 1, wherein the switch device is a diode, and comprising a first electrode layer disposed over the first n-doped layer and a second electrode disposed over the first p-doped layer.

3. A device as recited in claim 2, wherein the switch device is a p-i-n diode and the first n-doped layer comprises an n-drift portion forming the junction with the first p-doped layer and comprises an n-buffer layer between n-drift portion and the first electrode layer.

4. A device as recited in claim 1, wherein the switch device is a thyristor, the first p-doped layer being a p-base layer, and the first n-doped layer being an n-drift layer, and further comprising a semiconductor anode layer disposed on a side of the n-drift layer away from the switch blocking junction and a semiconductor cathode layer disposed on a side of the p-base layer away from the switch blocking junction.

5. A device as recited in claim 4, wherein the semiconductor anode layer has no edges forming the side wall of the groove.

6. A device as recited in claim 4, wherein the n-drift layer extends between the semiconductor anode layer and the side wall of the groove.

7. A device as recited in claim 4, wherein the n-drift layer includes an n-buffer layer.

8. A device as recited in claim 7, wherein the n-drift layer extends between the n-buffer layer and the side wall of the groove.

9. A device as recited in claim 7, wherein the semiconductor anode layer has no edges forming the side wall of the groove.

10. A device as recited in claim 9, wherein the n-drift layer extends between the n-buffer layer and the side wall of the groove.

11. A device as recited in claim 4, wherein the n-drift layer extends between the semiconductor anode layer and the groove wall.

12. A device as recited in claim 1, wherein the first n-doped layer comprises a high n-doped region and a low n-doped region between the high n-doped region and the first p-doped region, the switch blocking junction being formed between the low n-doped region and the first p-doped region, the low n-doped region extending between the high n-doped region and the groove.

13. A device as recited in claim 1, further comprising a light source disposed to direct light into the switch via the groove.

14. A device as recited in claim 13, wherein the light source comprises a light guide to couple light from the light source into the switch.

15. A device as recited in claim 14, wherein the light guide is disposed within the groove.

16. A device as recited in claim 13, wherein the light source is mounted to a plate positioned proximate the switch so as to illuminate the groove.

17. A device as recited in claim 16, wherein the groove enters the switch from a first side and the light source is disposed to the first side of the switch, wherein the light entering the switch from the light source is refracted at the side wall.

18. A device as recited in claim 17, wherein the switch comprises a window to permit light entering a second side of the switch opposing the first side to reflect light at the groove side wall.

19. A device as recited in claim 13, further comprising a plate disposed above the groove to reflect light from the light source to the semiconductor switch.

20. A device as recited in claim 19, wherein the plate comprises an electrically conducting material in electrical contact with an electrode of the semiconductor switch.

21. A device as recited in claim 19, wherein a lower surface of the plate facing the semiconductor switch contains a recess, the light source being at least partially contained within the recess.

22. A device as recited in claim 1, wherein the groove extends from the first n-doped layer into the first p-doped layer.

23. A device as recited in claim 1, wherein the groove is a V-groove.

24. A device as recited in claim 1, wherein the groove has sloped side walls and has a flat bottom portion.

25. A device as recited in claim 1, wherein the groove has sloped side walls and a rounded bottom portion.

26. A device as recited in claim 1, wherein the groove has first and second sloped walls, the first sloped wall forming a first angle with the switch axis and the second sloped wall forming a second angle with the switch axis, a magnitude of the first angle being different from a magnitude of the second angle.

27. A device as recited in claim 1, wherein the side wall lies at an angle relative to the switch axis of between 10° and 45°.

28. A device as recited in claim 1, further comprising a unit to generate light having an optical output coupled to a plurality of light guides, the light guides being coupled to illuminate the switch.

29. A device as recited in claim 28, wherein the light guides are associated with respective grooves on the switch.

30. A device as recited in claim 28, wherein the unit comprises a laser diode array and the light guides include optical fibers coupled to respective emitters of the laser diode array.

31. A device as recited in claim 1, wherein the switch comprises a beveled edge, light entering the switch in a direction substantially parallel to the

switch axis and being totally internally reflected by the beveled edge into the switch.

32. A method of controlling a semiconductor switch having a first p-doped layer and a first n-doped layer forming a switch blocking junction, the switch blocking junction being substantially perpendicular to a switch axis, the method comprising:

refracting light absorbable by the switch at a side wall of a groove in the switch, the side wall being disposed at least in the first n-doped layer and at a non-zero angle relative to the switch blocking junction and to the switch axis.

33. A method as recited in claim 32, further comprising reflecting light at the side wall.

34. A method as recited in claim 32, wherein directing the light further comprises totally internally reflecting light at a beveled edge of the switch.

35. A method as recited in claim 32, wherein the groove side wall extends from the first n-doped layer into the first p-doped layer.

36. A method as recited in claim 32, wherein the first n-doped layer comprises a first sub-layer having a relatively high n-doping and an second sub-layer having a relatively low n-doping, the switch blocking junction being formed between the second sub-layer and the first p-doped layer.

37. A light-activated semiconductor switch device, comprising:

a switch comprising a first n-doped layer and a first p-doped layer forming a switch blocking junction, the switch having an edge portion with a beveled edge surface; and

a light source directing light into the switch at the edge portion so as to internally reflect the light at the beveled edge surface.

38. A device as recited in claim 37, wherein the light source comprises an optical fiber disposed proximate the edge portion of the thyristor, the optical fiber emitting light through a fiber side to the edge portion.

39. A method of controlling a semiconductor switch having a switch blocking junction formed by a first p-doped layer and a first n-doped layer, the switch having a beveled edge, the method comprising:

passing light through a face of the semiconductor switch; and

totally internally reflecting the light by the beveled edge.

40. A method as recited in claim 39, further comprising passing the light through the side of an optical fiber to the face of the switch.

41. A light-activated thyristor device, comprising:

a thyristor comprising, in order from an anode side, a semiconductor anode layer, an n-doped layer, a p-doped layer and a semiconductor cathode layer, a groove extending into the thyristor through at least one of the anode layer and the cathode layer, wherein an edge of the at least one of the semiconductor anode layer and the semiconductor cathode layer through which the groove extends does not extend to a wall of the groove.

42. A device as recited in claim 41, wherein the n-doped layer is an n-drift layer and the p-doped layer is a p-base layer.

43. A device as recited in claim 42, wherein the n-drift layer extends between the anode layer and the groove.

44. A device as recited in claim 42, further comprising an anode electrode layer disposed on the semiconductor anode layer and a cathode electrode layer disposed on the semiconductor cathode layer.

45. A device as recited in claim 44, wherein the n-drift layer contacts a portion of the anode electrode layer proximate the groove.

46. A device as recited in claim 42, further comprising an n-doped buffer layer between the n-drift layer and the semiconductor anode layer.

47. A device as recited in claim 46, wherein the n-drift layer extends between the buffer layer and the groove.

48. A device as recited in claim 46, further comprising an anode electrode layer overlying the semiconductor anode layer, the electrode layer terminating, proximate the groove, above one of the buffer layer and the n-drift layer.

49. A device as recited in claim 41, wherein the p-doped layer is a p-drift layer and the n-doped layer is a n-base layer.

50. A device as recited in claim 49, wherein the p-drift layer extends between the semiconductor cathode layer and a groove wall.

51. A device as recited in claim 49, further comprising a cathode electrode layer disposed on the semiconductor cathode layer and an anode electrode layer disposed on the semiconductor anode layer.

52. A device as recited in claim 51, wherein the p-drift layer contacts a portion of the cathode electrode layer proximate a groove wall.

53. A device as recited in claim 49, further comprising a p-doped buffer layer between the p-drift layer and the semiconductor cathode layer.

54. A device as recited in claim 53, wherein the p-drift layer extends between the buffer layer and the groove wall.

55. A device as recited in claim 53, further comprising a cathode electrode layer overlying the semiconductor cathode layer, the cathode electrode layer terminating, proximate the groove, above one of the buffer layer and the p-drift layer.

56. A light activated semiconductor switch, comprising:

a first n-doped layer and a first p-doped layer forming a switch blocking junction, a groove having a light refracting side wall extending into one of the first n-doped and first p-doped layers from a side of the one of the first n-doped and first p-doped layers opposite from the switch blocking junction,

wherein, when the groove extends into the first n-doped region, the first n-doped layer comprises a high n-doped region separated from the first p-doped layer by a low n-doped region, the low n-doped region extending between the high n-doped region and the groove, and when the groove extends into the first p-doped region, the first p-doped layer comprises a high p-doped region separated from the first n-doped layer by a low p-doped region, the low p-doped region extending between the high p-doped region and the groove.

57. A switch as recited in claim 56, further comprising a first electrode layer overlying the first n-doped layer and a second electrode layer overlapping the first p-doped layer.

58. A switch as recited in claim 56, further comprising, when the groove extends into the first n-doped region, an anode semiconductor layer overlying the first n-doped layer, the groove extending through the anode semiconductor layer, and further comprising a semiconductor cathode layer on another side of the first p-doped layer from the switch blocking junction.

59. A switch as recited in claim 56, further comprising, when the groove extends into the first p-doped region, a cathode semiconductor layer overlying the first p-doped layer, the groove extending through the cathode semiconductor layer, and further comprising a semiconductor anode layer on another side of the first n-doped layer from the switch blocking junction.

60. A switch as recited in claim 56, further comprising a light source coupled to direct light through the groove wall.

61. A device as recited in claim 60, wherein the light source comprises a light guide to couple light from the light source into the switch.

62. A device as recited in claim 60, wherein the light source is mounted to a plate positioned proximate the switch so as to illuminate the groove.

63. A device as recited in claim 56, wherein the switch comprises a beveled edge, light entering the switch in a direction substantially parallel to the switch axis and being totally internally reflected by the beveled edge into the switch.

64. A light-activated semiconductor switch device, comprising:

a semiconductor switch comprising a first n-doped layer and a first p-doped layer forming a switch blocking junction, a groove having a light refracting side wall extending through one of the first n-doped layer and

the first p-doped layer into the other of the first n-doped layer and the first p-doped layer.

65. A device as recited in claim 64, wherein the switch device has a switch axis perpendicular to the blocking junction and at least a portion of the light refracting side wall is disposed non-parallel to the switch axis.

66. A device as recited in claim 64, wherein the switch device is a thyristor, and further comprising a semiconductor anode layer disposed on a side of the first n-doped layer away from the switch blocking junction and a semiconductor cathode layer disposed on a side of the first p-doped layer away from the switch blocking junction.

67. A device as recited in claim 66, wherein the semiconductor anode layer and the semiconductor cathode layer have no edges forming the side wall of the groove.

68. A device as recited in claim 64, wherein the first n-doped layer comprises a high n-doped region and a low n-doped region between the high n-doped region and the first p-doped region, the switch blocking junction being formed between the low n-doped region and the first p-doped region, the low n-doped region extending between the high n-doped region and the groove.

69. A device as recited in claim 64, wherein the first p-doped layer comprises a high p-doped region and a low p-doped region between the high p-doped region and the first n-doped region, the switch blocking junction being formed between the low p-doped region and the first n-doped region, the low p-doped region extending between the high p-doped region and the groove.

70. A device as recited in claim 64, further comprising a light source disposed to direct light into the switch via the groove.

71. A device as recited in claim 70, wherein the light source comprises a light guide to couple light from the light source into the switch.

72. A device as recited in claim 71, wherein the light guide is disposed within the groove.

73. A device as recited in claim 70, wherein the light source is mounted to a plate positioned proximate the switch so as to illuminate the groove.

74. A device as recited in claim 73, wherein the groove enters the switch from a first side and the light source is disposed to the first side of the switch, wherein the light entering the switch from the light source is refracted at the side wall.

75. A device as recited in claim 74, wherein the switch comprises a window to permit light entering a second side of the switch opposing the first side to reflect light at the groove side wall.

76. A device as recited in claim 70, wherein the light guide is disposed to illuminate the switch by totally internally reflecting light off a groove wall.

77. A device as recited in claim 70, further comprising a plate disposed above the groove to reflect light from the light source to the semiconductor switch.

78. A device as recited in claim 77, wherein the plate comprises an electrically conducting material in electrical contact with an electrode of the semiconductor switch.

79. A device as recited in claim 77, wherein a lower surface of the plate facing the semiconductor switch contains a recess, the light source being at least partially contained within the recess.

80. A device as recited in claim 64, wherein the groove is a V-groove.

81. A device as recited in claim 64, wherein the groove has sloped side walls and has a flat bottom portion.

82. A device as recited in claim 64, wherein the groove has sloped side walls and a rounded bottom portion.

83. A device as recited in claim 64, wherein the groove has first and second sloped walls, the first sloped wall forming a first angle with the switch axis and the second sloped wall forming a second angle with the switch axis, a magnitude of the first angle being different from a magnitude of the second angle.

84. A device as recited in claim 64, wherein the side wall lies at an angle relative to the switch axis of between 10° and 45°.

85. A device as recited in claim 64, further comprising a unit to generate light having an optical output coupled to a plurality of light guides, the light guides being coupled to illuminate the switch.

86. A device as recited in claim 85, wherein the light guides are associated with respective grooves on the switch.

87. A device as recited in claim 85, wherein the unit comprises a laser diode array and the light guides include optical fibers coupled to respective emitters of the laser diode array.

88. A device as recited in claim 64, wherein the switch comprises a beveled edge, light entering the switch in a direction substantially parallel to the switch axis and being totally internally reflected by the beveled edge into the switch.